IN THE CLAIMS:

Please cancel claims 9, 15, and 16. **Please also amend** claims 10, 11, and 13, and **add** new claims 19 and 20, as shown in the complete list of claims that is presented below.

Claims 1-4 (canceled).

Claim 5 (previously presented): A method for manufacturing a semiconductor device including:

a step of connecting, to one surface of a support semiconductor chip, first and second chip blocks each including one or a plurality of semiconductor chips having an active surface substantially parallel with the one surface of the support semiconductor chip;

a step of arranging an insulator between the first and second chip blocks; and

a step of forming, within or on a surface of the insulator, an intralevel wiring on a wiring plane as a plane including an inactive or active surface of any of the semiconductor chips constituting the first or second chip block.

Claim 6 (previously presented): A method for manufacturing a semiconductor device according to claim 5, wherein a plurality of semiconductor chips are present in the first chip block and a plurality of semiconductor chips are present in the second chip block, and wherein the active or inactive surface of one of the semiconductor chips in the first chip block and the active or inactive surface of one of the semiconductor chips in the second chip block are commonly on the wiring plane.

Claim 7 (previously presented): A method for manufacturing a semiconductor device according to claim 5, wherein the step of forming the intralevel wiring includes a step of forming first and second intralevel wirings respectively arranged on first and second wiring planes not in a same plane, and further including a step of forming an

interlevel wiring connecting between the first and second intralevel wirings.

Claim 8 (original): A method for manufacturing a semiconductor device according to claim 5, further including a step of forming a penetration hole in at least one of the semiconductor chips constituting the first and second chip blocks, and a step of arranging a conductor in the penetration hole.

Claim 9 (canceled).

Claim 10 (currently amended): A method for manufacturing a semiconductor device ~~according to claim 9,~~ including:

an on-substrate connecting step of connecting face down a semiconductor chip having an active surface with a recess and a conductor disposed in the recess onto one surface of a semiconductor substrate; and

a step of polishing or abrading an inactive surface of the semiconductor chip to expose the conductor at the inactive surface of the semiconductor chip after the on-substrate connecting step,

wherein the semiconductor substrate is a semiconductor wafer, wherein the semiconductor chip is a first semiconductor chip, wherein the on-substrate connecting step comprises arranging and connecting the first semiconductor chip and a second semiconductor chip side by side on the semiconductor wafer, and further including a step of cutting the semiconductor wafer based on a predetermined region that includes at least one of the first and second semiconductor chips to obtain a semiconductor device having a chip-on-chip structure.

Claim 11 (currently amended): A method for manufacturing a semiconductor device ~~according to claim 9,~~including:

an on-substrate connecting step of connecting face down a semiconductor chip having an active surface with a recess and a conductor disposed in the recess onto one surface of a semiconductor substrate; and

a step of polishing or abrading an inactive surface of the semiconductor chip to

expose the conductor at the inactive surface of the semiconductor chip after the on-substrate connecting step,

wherein the one surface of the semiconductor substrate is an active surface, and further including a substrate polish step of polishing or abrading the inactive surface of the semiconductor substrate to reduce the thickness thereof.

Claim 12 (previously presented): A method for manufacturing a semiconductor device according to claim 11, wherein the active surface of the semiconductor substrate has a recess with a conductor therein, the substrate polish step including a step of polishing or abrading the inactive surface of the semiconductor substrate to expose the conductor at the inactive surface of the semiconductor substrate.

Claim 13 (currently amended): A method according to claim ~~9~~ 10, further including an on-chip connecting step of connecting, on the semiconductor chip, another semiconductor chip.

Claim 14 (previously presented): A method according to claim 13, wherein the other semiconductor chip has an active surface with a recess having a conductor therein, the on-chip connecting step being to connect face down the other semiconductor chip on the semiconductor chip, and further including a step of polishing or abrading an inactive surface of the other semiconductor chip to expose the conductor of the other semiconductor chip ~~in~~ at the inactive surface of the other semiconductor chip.

Claims 15-18 (canceled).

Claim 19 (new): A method according to claim 11, further including an on-chip connecting step of connecting, on the semiconductor chip, another semiconductor chip.

Claim 20 (new): A method according to claim 19, wherein the other semiconductor chip has an active surface with a recess having a conductor therein, the on-chip connecting step being to connect face down the other semiconductor chip on the

semiconductor chip, and further including a step of polishing or abrading an inactive surface of the other semiconductor chip to expose the conductor of the other semiconductor chip at the inactive surface of the other semiconductor chip